Shurong Cao

PhD Student in Electronic Engineering | The Chinese University of Hong Kong

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Education & Research Direction

The Chinese University of Hong Kong — PhD in Electronic Engineering, 2026–present
Supervisor: Prof. Ni Zhao. Exploring semiconductor devices and fabrication for BEOL-compatible and monolithic 3D electronics, including low-temperature processing, oxide and p-type semiconductors, and complementary integration.

Nanjing University — B.Eng. in Integrated Circuit and System Design, 2022–2026
School of Integrated Circuits, Suzhou Campus. Undergraduate thesis: *Parameter Optimization of Nano-TSVs for 3D Integrated Circuits.*

Publications

FALCO-WAFER: Feature-Aware Lightweight Contextual Detector for Wafer Defect Detection
Haotian Zhang*, **Shurong Cao***, Ningmu Zou
IEEE International Test Conference in Asia (ITC-Asia), pp. 43–47, 2025.
DOI: 10.1109/ITC-Asia67627.2025.00016

Texture-AD: An Anomaly Detection Dataset and Benchmark for Real Algorithm Development
Tianwu Lei*, Bohan Wang*, Silin Chen, **Shurong Cao**, Ningmu Zou
arXiv:2409.06367, 2024 · CVM 2026 conference program.

Selected Research & Engineering

Advanced packaging and nano-TSV modeling. Developed Python-assisted equivalent-material modeling workflows and thermo-mechanical simulations of 2.5D chip stacks using COMSOL and ANSYS at Nanjing University.

Vacuum MOSFET sensing. Worked on COMSOL model development, device architecture refinement, simulation verification, and model integration in a national-level undergraduate innovation project. Co-inventor of granted Chinese patent CN120352074B (2025).

Research exchange at HKUST (Guangzhou). Modeled optical neuromemristors and nano-antennas, explored geometry optimization, and participated in device-characterization work.

FPGA robotic system. Integrated PYNQ-Z2, Raspberry Pi 5, and STM32 hardware, with electronic-module assembly, wireless motion control, radar-based SLAM, and IMU drift compensation.

Open-Source Engineering

BenchLineage maintainer. Research provenance, calibration records, uncertainty budgets, evidence bundles, and ELN archive interoperability. Related contributions were integrated into the ELN format checks and eLabFTW importer tests.

Upstream contributor. 37 merged pull requests across 22 external repositories, including Astropy, cibuildwheel, the ELN File Format, and GitHub MCP Server (GitHub snapshot: 11 September 2026).

Recognition & Communication

Guo Xie Birong Scholarship. Nanjing University, RMB 10,000.
National Second Prize, 2024. FPGA Innovation Design Track Finals, 7th National College Embedded Chip and System Design Competition.
Team leader and commencement speaker. Hardware design program at St Catharine’s College, Cambridge.

Technical Background

Semiconductor-device modeling; COMSOL and ANSYS; Python, C, PyTorch, Git and Linux; Verilog, FPGA, STM32, ROS and embedded systems. Mandarin and English.